(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 162 677 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 85303488.2

(22) Date of filing: 17.05.85

(51) Int. Cl.⁴: H 01 L 21/00
H 01 L 21/82, H 01 L 27/15

(30) Priority: 18.05.84 JP 98542/84
18.05.84 JP 98543/84
18.05.84 JP 98544/84
19.05.84 JP 99691/84
29.06.84 JP 133298/84

(43) Date of publication of application: 27.11.85 Bulletin 85/48

(84) Designated Contracting States: DE FR GB

(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Wada, Osamu
10-11, Takamoridai 2-chome
Isehara-shi Kanagawa 259-11(JP)

(72) Inventor: Sanada, Tatsuyuki
6-9-301, Susukino 3-chome Midori-ku
Yokohama-shi Kanagawa 227(JP)

(72) Inventor: Miura, Shuichi
Nakamura Haitsu 302 1945, Okada
Atsugi-shi Kanagawa 243(JP)

(72) Inventor: Machida, Hideki
Fujitsu Atsugi-ryo 3-10, Sakae-cho, 2-chome
Atsugi-shi Kanagawa 243(JP)

(72) Inventor: Yamakoshi, Shigenobu
Ebina Danchi 1-601 117, Nakaniida
Ebina-shi Kanagawa 243-04(JP)

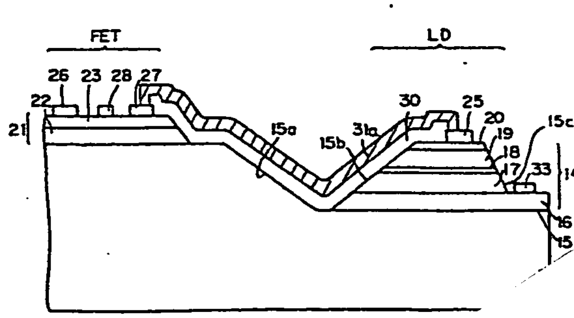
(72) Inventor: Sakurai, Teruo
18-6, Yokodai 3-chome
Sagamihara-shi Kanagawa 229(JP)

(74) Representative: Fane, Christopher Robin King et al,
HASELTINE LAKE & CO. Hazlitt House 28 Southampton Buildings Chancery Lane
London, WC2A 1AT(GB)

(54) Semiconductor device and method for producing same.

(57) A semiconductor device includes a substrate (1) having a low substrate surface (15) formed in the substrate with a first gentle slope (15a) from the substrate surface and a single crystalline layer formed on the low substrate surface nearly level with the substrate surface and having a gentle slope (15b) facing the first gentle slope. An optical semiconductor element (LD) is constructed using the single crystalline layer and an electronic semiconductor element (FET) is constructed using the substrate surface. A wiring layer (31a) connects electrodes (25, 27) of the optical semiconductor element (LD) and the electronic semiconductor element (FET) through the first and the second gentle slopes, the slopes being gentle enough to reduce breakage of the wiring which can occur when steeper slopes, produced by conventional methods, are used.

Fig.2



EP 0 162 677 A2

0162677

SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING SAME

The present invention relates to a semiconductor device and a method for producing the same.

Recent advances in the technologies of crystal growth and device production have made it possible to combine optical and electronic devices into a single chip. Such an optoelectronic integrated circuit (OEIC) is not only smaller and easier to use in various systems but also speedier, more reliable, and less noisy than hybridized discrete devices. A particular attractive and important OEIC is one wherein an optical semiconductor element, for example, a laser diode or photo diode (PD), is monolithically integrated with a field effect transistor (FET) driver.

In fabricating a laser/FET unit or PD/FET unit, there is a problem in how to match the laser structure to the FET structure, as each component has a very different layer structure. A laser has a higher structure than FET's. As conventional photolithographic technology requires a wafer with an even surface, the laser must therefore be formed in an etched groove. Assuming the substrate is of a (100) oriented semi-insulating GaAs substrate, when the substrate is chemically etched, a $(01\bar{1})$ face is exposed as a side wall and the $(01\bar{1})$ face forms a 55° angle with respect to the (100) top surface so that a groove having a sharp step is formed. This sharp step itself, however, makes application of the photolithographic technology difficult. Thus, high integration of the laser/FET unit

becomes difficult.

Further, the sharp 55° angle step often results in breakage of wiring and thus a reduced production yield.

It is therefore desirable, in view of the above disadvantages of the prior art, to provide a method for producing a semiconductor device wherein both optical semiconductor elements, such as a laser diode, and ordinary electronic semiconductor elements, such as an FET, are formed nearly flatly on a single substrate.

It is also desirable to provide a semiconductor device wherein an optical semiconductor element/ordinary semiconductor unit is formed on a single substrate with high integration.

According to one aspect of the present invention, there is provided a method for producing a semiconductor device including the steps of: forming a low substrate surface in a substrate with a gentle slope from the substrate surface; forming on the low substrate surface a single crystalline layer substantially level with the substrate surface; forming an optical semiconductor element and an electronic semiconductor element using the single crystalline layer and the substrate surface, respectively; and forming a wiring layer connecting the optical semiconductor element and the electronic semiconductor element on the gentle slope.

According to another aspect of the present invention, there is provided a semiconductor device including: a substrate having a low substrate surface formed in the substrate with a first gentle slope from the substrate surface; a single crystalline layer formed on the substrate surface nearly level with the substrate surface and having a second gentle slope facing the first gentle slope; an optical semiconductor element is

constructed using the single crystalline layer. An electronic semiconductor element is constructed using the substrate surface. A wiring layer connects electrodes of the optical semiconductor element and the electronic semiconductor element through the first and the second gentle slopes.

According to yet another aspect the present invention, there is provided a method for producing a semiconductor device including the steps of: forming a substrate; forming a low substrate surface in the substrate surface with a first gentle slope from the substrate surface; forming on the low substrate surface a single crystalline layer nearly level with the substrate surface; forming in the single crystalline layer a second gentle slope facing the first gentle slope; forming an optical semiconductor element using the single crystalline layer; forming an electronic semiconductor element using the substrate surface; and forming a wiring layer connecting the electrodes of the optical semiconductor element and the semiconductor element through the first and the second gentle slopes.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Figures 1A to 1K show cross-sectional views for explaining an embodiment of a method for producing a semiconductor device according to the present invention.

Figs.2 and 3 show partially enlarged cross-sectional views of Fig. 1K;

Fig. 4 shows a perspective view of Fig. 1K;

Fig. 5 is a schematic circuit diagram of the devices of Fig. 4;

Fig. 6 shows a cross-sectional view for explaining an embodiment of a semiconductor device according to the present invention;

Fig. 7 is a schematic circuit diagram of the device of Fig. 6;

Fig. 8 shows a cross-sectional view of another embodiment of a device according to the present invention;

Fig. 9 shows a perspective view relating to Fig. 8;

Fig. 10 is a schematic circuit diagram of the device of Fig. 9;

Figs. 11A and 11B show cross-sectional views for explaining an embodiment of a method for forming a gentle step in a substrate;

Figs. 12A and 12B show cross-sectional views for explaining another embodiment of a method for forming a gentle step in a substrate;

Fig. 13A and 13B show cross-section views for explaining still another embodiment of a method for forming a gentle step in a substrate.

Figures 1A to 1K are cross-sectional views for explaining an embodiment of a method for producing a semiconductor device according to the present invention.

After providing a GaAs substrate 1 as shown in Fig. 1A, a photo resist 2, for example, AZ4620 (produced by Hoechst), having a thickness of 5 to 15 μm is formed over the surface of the GaAs substrate 1 and patterned in a stripe form, as shown in Fig. 1B.

The width W of the stripes of the resist layer may be 50 to 200 μm, preferably 100 μm. And the thickness d may be 7 ∿ 8 μm.

Next, as shown in Fig. 1C, heat treatment for baking is carried out for 10 minutes at a temperature of 200°C to change the edges of the resist layer 2 to gentle slopes and increase the thickness d' of the resist layer 2 to about 8 to 10 μm. In this heat treatment, the temperature is 200°C which is lower than the usual post baking temperature 120°C. And the width W will not be changed so that the slope α of the edge of the mask 2 is approximately 5° ∿ 15°. The thickness d' of the resist mask should be larger than the total thickness of the semiconductor laser layer which will be formed in a

groove later. There are some rules which decide the slope of the heated mask. That is, one relationship between W and d corresponds to one slope of the edge.

As shown in Fig. 1D, a resist layer 3 is formed over the obtained structure and then patterned. The patterned resist layer 3 has a thickness of 5 to 15 μm. Since the resist layer 2 had been heat-treated, it is not removed in the patterning process of the resist layer 3. Thus, the gentle slopes of the resist layer 2 facing the center in of Fig. 1D are exposed, while the other slopes are protected by the resist layer 3. A slight heat-treatment is carried out to dry the patterned resist layer 3.

As shown in Fig. 1E, an ion beam etching, for example, argon ion (Ar^+) beam etching, is used to etch a mesa while rotating the GaAs substrate 1. In this ion beam etching process, the ion beam irradiates the GaAs substrate 1 at an angle of about 70°. When the mesa height h is about 10 μm, the ion beam etching process is ended. Thus, a groove 4 having a slope 12 at an angle α of about 5° to 15° is formed in the GaAs substrate 1. The ion beam etching conditions are an acceleration voltage of 500 and an ion current density of 0.57 mA/cm^2. That is, the ion beam etching process etches all of the surface of the substrate equally, irrespectively of the various materials thereof. As a result, the surface shape of the mask 2,3 is shifted to the surface of the etched substrate 1.

As shown in Fig. 1F, the resist layers 2 and 3 are then removed, resulting in a GaAs substrate 1 having a mesa type recess or groove 4 with a gentle slope 12.

As shown in Fig. 1G, a semiconductor laser layer 5 consisting of an n^+ type GaAs layer, n type $Al_{0.3}Ga_{0.7}As$ layer, etc. is grown over the entire the GaAs substrate 1 by molecular-beam epitaxy (MBE). The structure of the layers corresponds to that of the optical semiconductor element, i.c. LD, also possible as PD.

As shown in Fig. 1H, the semiconductor laser layer 5 is then patterned using two above-mentioned gentle-slope forming steps, which is shown as the mask 2,3 in Fig. 1G.

As shown in Fig. 1I an SiO_2 layer 7 is formed over the obtained structure and then patterned so that the SiO_2 layer covers the layer 5 formed in the etched groove. Then an FET epitaxial layer 8 is grown on the substrate while forming a polycrystalline (Al)GaAs layer 9 on the SiO_2 layer 7. The structure of the FET epitaxial layer 8 corresponds to that of a FET the thickness of which is not so large as the semiconductor laser layer 5.

As shown in Fig. 1J, the polycrystalline (Al)GaAs layer 9 is removed by a chemical etching process using a resist layer 10 as a mask. After that, the SiO_2 layer 7 is also etched and the resist layer 10 is removed. Then, various LD and FET electrodes and a wiring layer 11a, 11b are formed on the gentle slope 12 as shown in Fig. 1K.

The reasons for making the gentle slope 12 depend on two main requirements which are necessary for making the OEIC.

Firstly, in order to deposit the wiring layer on the slope between LD and FET, the slope should be gentle because it is quite difficult to deposit a thick enough wiring layer on a sharp slope as used conventionally.

Secondly, in the patterning process of the wiring layer 11a, 11b formed on the entire surface of the substrate, a photo resist layer should be coated on the wiring layer. The thickness of the coating resist layer should be large enough to cover properly even on the sharp slope. This means the thickness of the resist coated on the upper surface where the FET's wiring is patterned becomes thick. This makes it impossible to make a fine pattern for the FET IC because of the thick resist. However, according to an embodiment of the present inven-

tion, since the slope is gentle, the coating resist can be thin and it is possible to make a fine pattern.

A detailed explanation relating to Fig. 1K will be given below.

Figure 2 shows a partially enlarged cross-sectional view of Fig. 1K, illustrating an embodiment of a structure according to the present invention. In Fig. 2, reference numeral 1 represents the GaAs substrate, 14 the semiconductor laser layer structure which is multi-layer, 15 a recess, 15a, 15b and 15c gentle slopes, 16 an n side contact layer of an n^+ type GaAs, 17 an n side clad layer of n type $Al_{0.3}Ga_{0.7}As$, 18 an active layer of either n type or p-type GaAs, 19 a p side clad layer of p type $Al_{0.3}Ga_{0.7}As$, 20 a p side contact layer of p^+ type GaAs, 21 an FET layer, 22 an undoped GaAs layer, 23 an n GaAs FET active layer, 25 a p side contact electrode of AuZn, 26 a source electrode of AuGe/Ni, 27 a drain electrode of AuGe/Ni, 28 a gate electrode of Al, 30 an insulating layer of SiO_2 , and 31 a wiring layer of Au/Cr. Although in Fig. 1K there is a step on the left hand side gentle slope, it is possible not to form such a step as shown at the gentle slope 15b in Fig. 2.

A method for producing the structure of Fig. 2 in which the p side contact electrode 25 is connected to the drain electrode 27 through the wiring layer formed on the gentle slopes 15a and 15b, will be explained below in detail.

After forming a recess 15 having the gentle slopes 15a as explained above, the n side contact layer 16, the n side clad layer 17, the active layer 18, the p side clad layer 19 and the p side contact layer 20 are successively formed. The multilayer 14 consisting of the n side contact layer 16 to the p side contact layer 20 is patterned by the above-mentioned gentle-slope forming process.

Then, the FET layer 21 consisting of the undoped

GaAs layer 22 and n GaAs active layer 23 is formed by MBE, as explained above with reference to Figs. 1I, 1J.

The p side contact electrode 25 for the LD is then formed on the p side contact layer 20 by a lift-off process.

After that, the n side contact electrode 33 is formed on the n side contact by a lift-off process and an alloying.

The source electrode 26 and the drain electrode 27 for the FET are also formed on the FET layer 21.

The insulating layer 30 is formed over the obtained structure by a sputtering process and is patterned by photolithography.

A wiring layer 31a is formed on the gentle slope 15a, 15b via the insulating layer 30 by a lift-off process.

Thus, the structure of Fig. 2 can be formed on a single GaAs substrate.

Figure 3 shows another partial enlarged cross-sectional view of Figure 1K. In Fig. 3, the same reference numerals as in Fig. 2 represent the same portions.

As seen from the figure, the source electrode 26 is connected to the n side contact electrode 33 through the wiring 31b formed on the gentle slope 15d via the insulator layer 30.

Figure 4 shows a perspective view relating to Fig. 1K, Fig. 1K being a cross-sectional view taken along the AA line.

Figure 5 is a circuit diagram of the device of Fig. 4.

As easily understood from the accordance between the Fig. 4 and Fig. 5, the wiring 31a on the gentle slopes 15a, 15b connects between the LD and the FET Q_2, and the wiring 31b on the gentle slope 15d connects between the LD and the FET Q_1. In this embodiment, the LD and Q_2 can be connected by the wiring 31a formed in OEIC so that the characteristic of the OEIC is

improved.

Figure 6A shows a cross-sectional view for explaining another embodiment of a semiconductor device according to the present invention. In Fig. 6A, the LD and FET are also formed on a GaAs substrate 1. The drain electrode 27 is connected to the p side contact electrode 25 via the wiring 31c formed on the planer surface.

The process of this embodiment is almost same as the process shown in Fig. 1A-1H. That is, as shown in Fig. 6B, after forming the semiconductor laser layer 5, the combination mask 2 and 3 is formed so that the edge of the mask 2,3 corresponds to the slope of the layer 5 (shown 5a). After that the planer surface 32 can be formed on the gentle slope 15a by performing the ion beam etching process as explained above.

The same reference numerals as in Fig. 2 and 3 represent the same portions. Figure 7 is a schematic circuit diagram of the device of Fig. 6.

Figure 8 shows a cross-sectional view of another embodiment of a device according to the present invention. In Fig. 8, a pin photo-diode (PIN PD) and an FET are formed on a single semi-insulating GaAs substrate 1. In Fig. 8, reference numeral 40 is an n^+ type GaAs layer, 41 an n^- type GaAs layer, 42 a high resistivity $Al_{0.3}Ga_{0.7}As$ layer, 43 a Zn diffused region, 45 an Si_3N_4 layer, 46 an undoped GaAs layer, 47 an n type GaAs layer, 48 an Al electrode, 50 a wiring layer of Au/Ti, 51 an Au/AuGe electrode, and 52 an Au/Zn/Au electrode. As shown in Fig. 8, the Al electrode 48 is interconnected to the Au/Zn/Au electrode through an Au/Ti wiring layer 50 continuously laid on the gentle slopes 15a and 15b.

Figure 9 shows a perspective view of the device of Fig. 8 which is a cross sectional view of B-B.

Figure 10 is a circuit diagram of the device of Fig. 9.

Other methods for forming a recess having a

gentle slope in a semi-insulating GaAs substrate will now be explained. Figures 11A and 11B show cross-sectional views of an embodiment explaining one of the methods. As shown in Fig. 11A, a resist layer 61 having a thickness of, for example, 6 μm is formed. The resist layer 61 is then exposed through a mask of a photo-sensitive glass having a hole 64 with a taper wall and a glass fiber 63. The resist layer just under the glass fiber 63 is most exposed, and as the distance is larger from the position on the resist layer just under the glass fiber, the amount of exposure is gradually reduced.

Thus, as shown in Fig. 11B, the resist layer has a pattern 66 having a gentle slope 65.

After that, using ion etching or reactive ion etching, the entire surface of the obtained structure is etched. Thus, a recess having the same pattern 66 can be formed in the semi-insulating GaAs substrate 1.

Figures 12A and 12B show cross-sectional views for explaining another embodiment of a method for forming a gentle slope in a substrate. As shown in Fig. 12A, a polyimide layer having a thickness of, for example, 6 μm is formed on a semi-insulating GaAs substrate 1. The polyimide layer is irradiated with a laser so that a portion of the polyimide in which a recess having a gentle slope is formed is irradiated less compared to the surrounding portion. The center of the recess forming portion may be not irradiated at all. After that, the recess forming process for the semi-insulating GaAs substrate is carried out as explained with Fig. 11B.

Figures 13A and 13B show cross-sectional views of another embodiment explaining a method for forming a gentle slope in a substrate. As shown in Fig. 13A, a first polyimide resin layer 72_1 having a thickness of, for example, 6000Å (0.6μm) is formed on a semi-insulating GaAs substrate 1. Then, the first polyimide resin layer 72_1 is heat-treated at a first temperature T_1 of, for example, 200°C. A second polyimide resin layer 72_2 is

formed on the first polyimide resin layer 72_1 and is heat-treated at a second temperature T_2 of, for example, 180°C, lower than the first temperature T_1. The process is repeated until the nth polyimide layer is formed on the (n-1)th polyimide layer and is heat-treated at a temperature T_n lower than temperature T_{n-1}. Thus, a polyimide resin multi-layer 72 is formed on the semi-insulating GaAs substrate. When a polyimide resin is heat-treated at a higher temperature, the etching rate is decreased.

Then, as shown in Fig. 13B the polyimide resin multilayer 72 is etched by an etchant, using a resist layer 73 having an opening 74 as a mask so that a recess 75 having a gentle slope 76 is formed in the polyimide multilayer 72. Then, the recess forming process as explained in Fig. 11B. is carried out for the semi-insulating GaAs substrate.

Furthermore, another embodiment will be explained by using the Fig. 13A, 13B. In this embodiment, the multi-layer 72_1 , 72_2 ... 72_n comprises $Al_xGa_{1-x}As$ layers in which the x is gradually increased from 72_1 to 72_n. Then, the wet etching process using a etchant containing HF is performed so that since the AlGaAs is etched faster than the GaAs or AlGaAs with surall quantity of Al, the etched pattern becomes shown in Fig. 13B having a gentle slope 76. After that, there are two alternative processes. The first process is that the ion beam etching is simply performed in the same manner as the previous explained process. The second process is that since the multi-layer 72 comprises a AlGaAs compound semiconductor, the FET structure is formed on or in the multi-layer 72.

CLAIMS

1. A method for producing a semiconductor device, comprising

the steps of:

forming a low substrate surface in a substrate with a gentle slope from the substrate surface;

forming on the low substate surface a single crystalline layer substantially level with the substrate surface;

forming an optical semiconductor element and an electronic semiconductor element using the single crystalline layer and the substrate surface, respectively; and

forming a wiring layer connecting the optical semiconductor element and the electronic semiconductor element on the gentle slope.

2. A method according to claim 1, wherein said substrate is semi-insulating GaAs.

3. A method according to claim 1, wherein said gentle slope is formed on said substrate by the steps of:

forming a first resist layer on said substrate in a stripe form;

subjecting the stripe-shaped resist layer to heat-treatment so that the edges of the stripe-shaped resist layer are rounded;

covering the substrate and stripe-shaped resist layer on regions other than where the gentle slope is to be formed at one side; and

etching the exposed substrate by ion beam etching.

4. A method according to claim 1, wherein said gentle slope is formed on said substrate by the steps of:

forming a resist layer on said substate and exposing the resist layer using a mask having optical properties which disperse or collect light.

5. A method according to claim 4, wherein said mask is composed of photo-sensitive glass having a tapered hole and an optical fiber arranged in the tapered hole.

6. A method according to claim 1, wherein said gentle slope is formed on said substrate by the steps of:

forming a polyimide resin layer on said substrate;

subjecting the polyimide resin layer to heat-treatment having a local temperature distribution;

patterning the heat-treated polyimide resin layer to make a recess having a gentle slope through a mask; and

patterning the substrate by the dry-etching process.

7. A method according to claim 1, wherein said gentle slope is formed on said substrate by a method comprising the steps of:

forming a polyimide resin multilayer obtained by forming a first polyimide resin layer heat-treated at first temperature on the substrate a second polyimide resin layer heat-treated at a second temperature lower than the first temperature, and so on;

patterning the polyimide resin multilayer through a mask to make a recess having a gentle slope; and

patterning the substrate by the dry-etching process.

8. A method according to claim 6 or 7, wherein said dry-etching is ion beam etching or reactive ion etching.

9. A method according to claim 1, wherein said optical semiconductor element is a laser diode or a photo-diode.

10. A method according to claim 1, wherein said

electronic semiconductor element is a field effect transistor.

11. A semiconductor device including:

a substrate having a low substrate surface formed in the substrate with a first gentle slope from the substrate surface;

a single crystalline layer formed on the low substrate surface nearly level with the substrate surface and having a second gentle slope facing the first gentle slope;

an optical semiconductor element being constructed using the single crystalline layer;

an electronic semiconductor element being constructed using the substrate surface; and

a wiring layer connecting electrodes of the optical semiconductor element and the electronic semiconductor element through the first and the second gentle slope.

12. A semiconductor device according to claim 11, wherein said optical semiconductor element is a laser diode or a photo-diode.

13. A semiconductor device according to claim 11, wherein said electronic semiconductor element is a field effect transistor.

14. A method for producing a semiconductor device comprising the steps of:

forming a substrate;

forming a low substrate surface in the substrate surface with a first gentle slope from the substrate surface;

forming on the low substrate surface a single crystalline layer nearly level with the substrate surface;

forming in the single crystalline layer a second gentle slope facing the first gentle slope;

forming an optical semiconductor element using the single crystalline layer;

forming an electronic semiconductor element using the substrate surface; and

forming a wiring layer connecting the electrode of the optical semiconductor element and the semiconductor element through the first and the second gentle slope.

15. A method according to claim 14 , wherein said substrate is semi-insulating GaAs.

16. A method according to claim 14, wherein said gentle slope is formed on said substrate by a method comprising the steps of:

forming a first resist layer on said substrate in a stripe form;

subjecting the stripe-shaped resist layer to heat-treatment so that the edge of the stripe-shaped resist layer are rounded;

covering the substrate and stripe-shaped resist layer on regions other than where the gentle slope is to be formed; and

etching the exposed substrate by ion beam etching.

17. A method according to claim 14, wherein said gentle slope is formed on said substrate by the steps of:

forming a resist layer on said substrate and

and exposing the resist layer using a mask having optical properties which disperse or collect light.

18. A method according to claim 17, wherein said mask is composed of photo-sensitive glass having a tapered hole and an optical fiber arranged in the tapered hole.

19. A method according to claim 14, wherein said gentle slope is formed on said substrate by the steps of:

forming a polyimide resin layer on said substrate,

subjecting the polyimide resin layer to a

heat-treatment having a local temperature distribution; patterning the heat treated polyimide resin layer to make a recess having a gentle slope through a mask; and patterning the substrate by the dry-etching process.

20. A method according to claim 14, wherein said gentle slope is formed on said substrate by a method comprising the steps of:

forming a polyimide resin multilayer obtained by forming a first polyimide resin layer heat-treated at a temperature on the substrate, a second polyimide resin layer heat-treated at a second temperature lower than the first at temperature, and so on;

patterning the polyimide resin multilayer through a mask to make a recess having a gentle slope; and

patterning the substrate by the dry-etching process.

21. A method according to claim 19 or 20, wherein said dry-etching is ion beam etching or reactive ion etching.

22. A method according to claim 14, wherein said optical semiconductor element is a laser diode or a photo-diode.

23. A method according to claim 14, wherein said electronic semiconductor element is a field effect transistor.

Fig. 1A

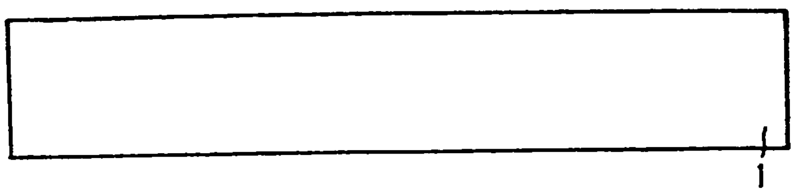


Fig. 1B

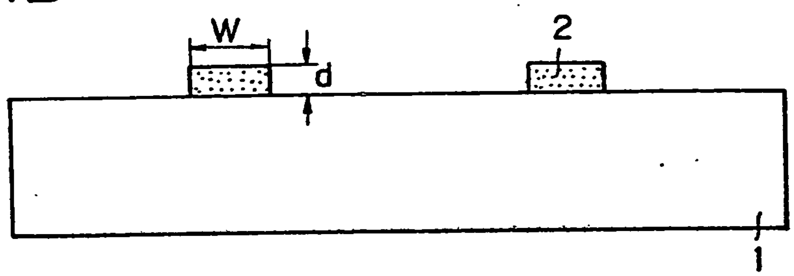


Fig. 1C

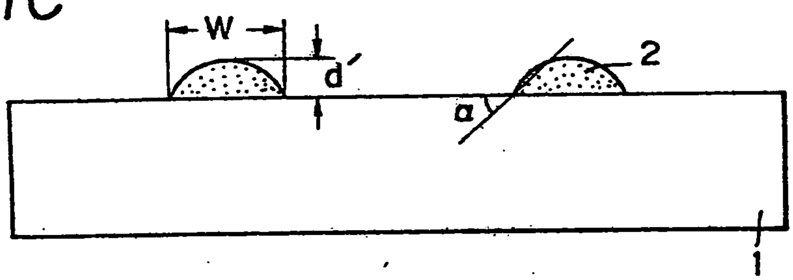


Fig. 1D

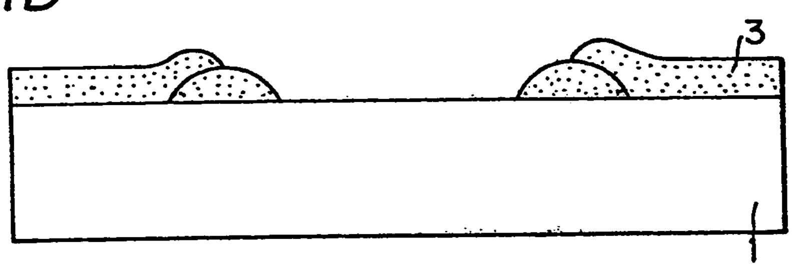


Fig.1E

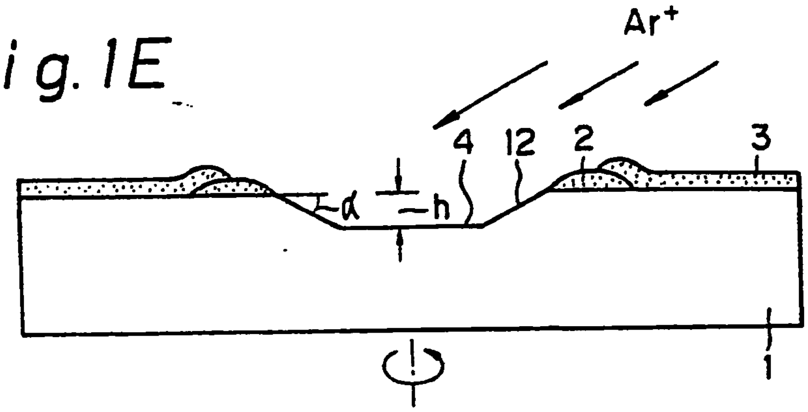


Fig.1F

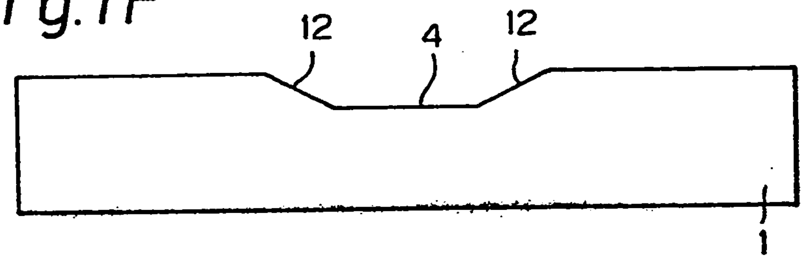


Fig.1G

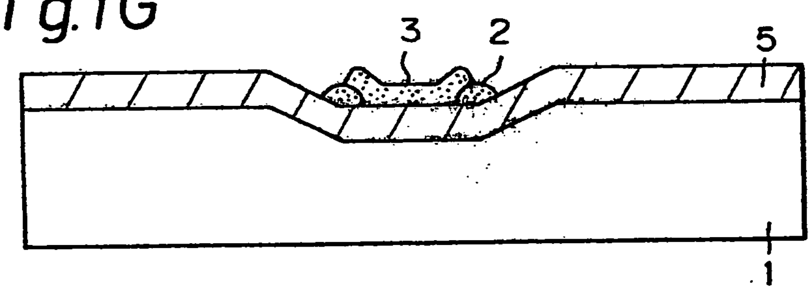
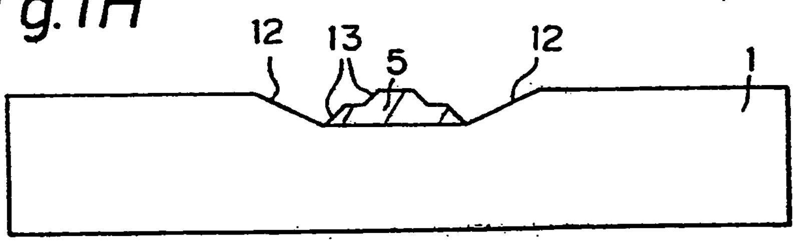


Fig.1H



0162677

Fig.1I

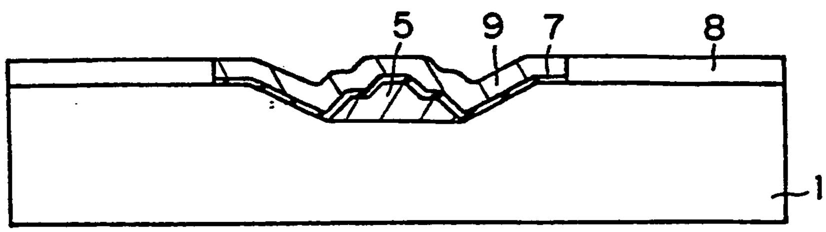


Fig.1J

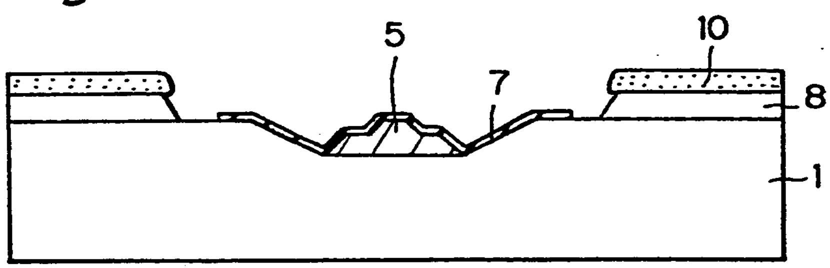


Fig.1K

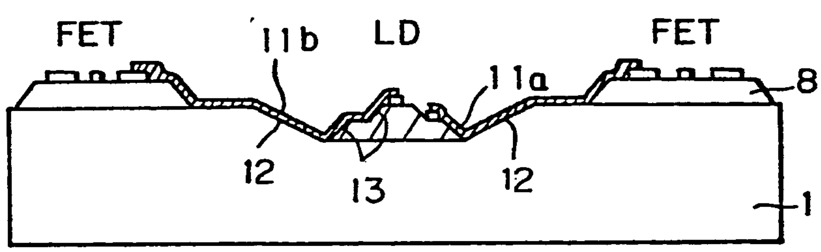
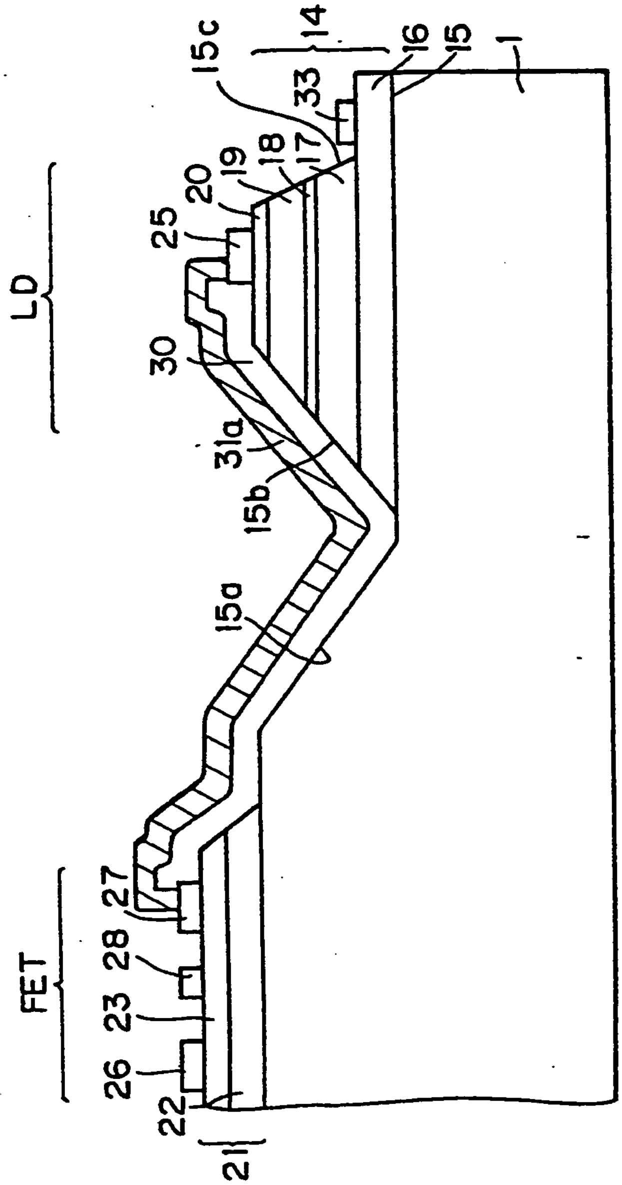
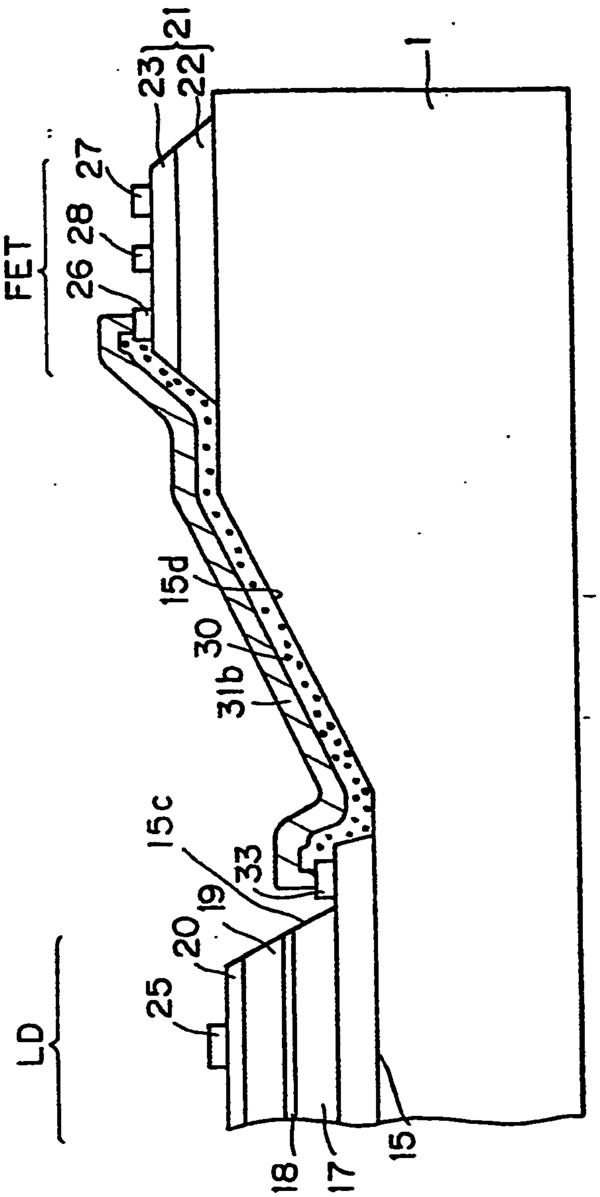


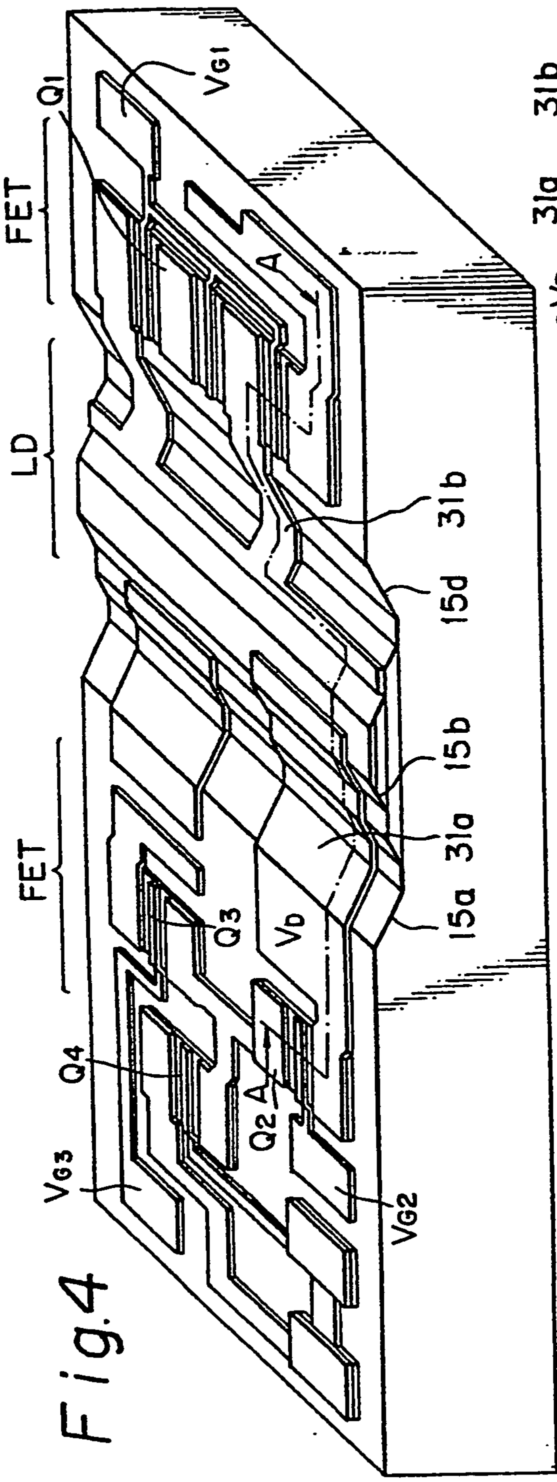
Fig.2



LD
FET
14
15c
16
15
1
33
17
18
19
20
25
30
31a
15b
15a
27
28
23
26
22
21

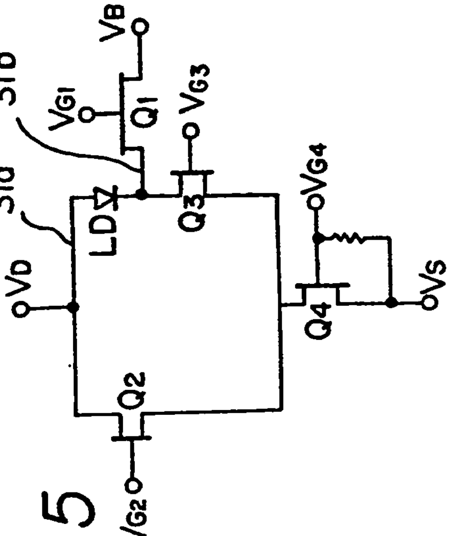
Fig.3





Q1
V_{G1}
FET
LD
FET
A
31b
15d
15b
31a
15a
Q3
V_D
Q4
Q2
A
V_{G3}
V_{G2}

Fig.4



V_B
V_{G1}
Q1
V_{G3}
31b
31a
LD
Q3
V_{G4}
V_D
V_S
Q4
Q2
V_{G2}

Fig.5

Fig. 6A

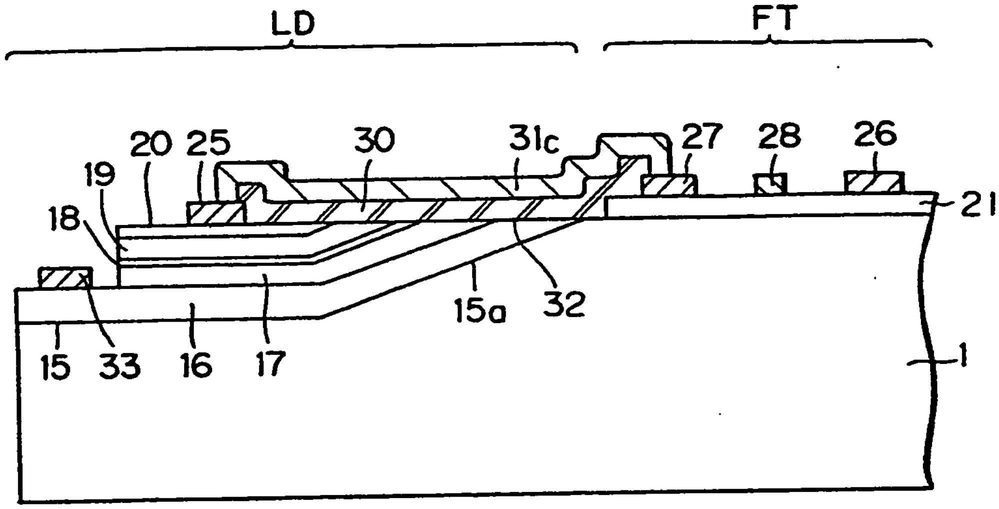


Fig. 6B

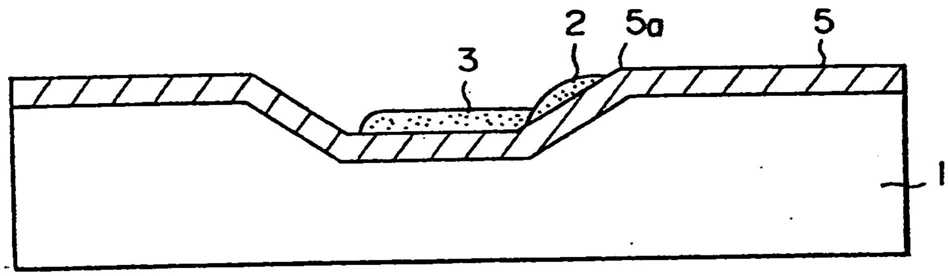


Fig.7

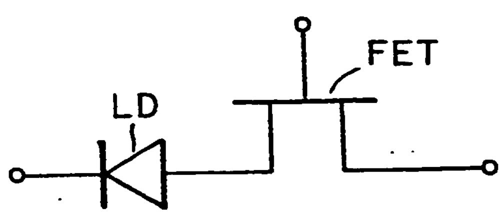
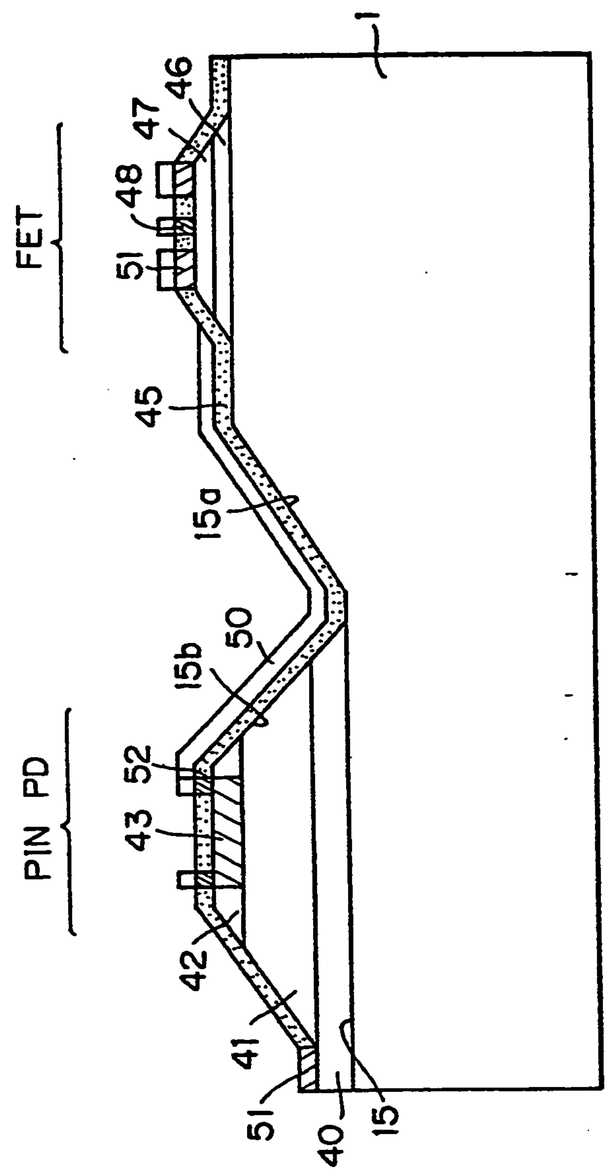
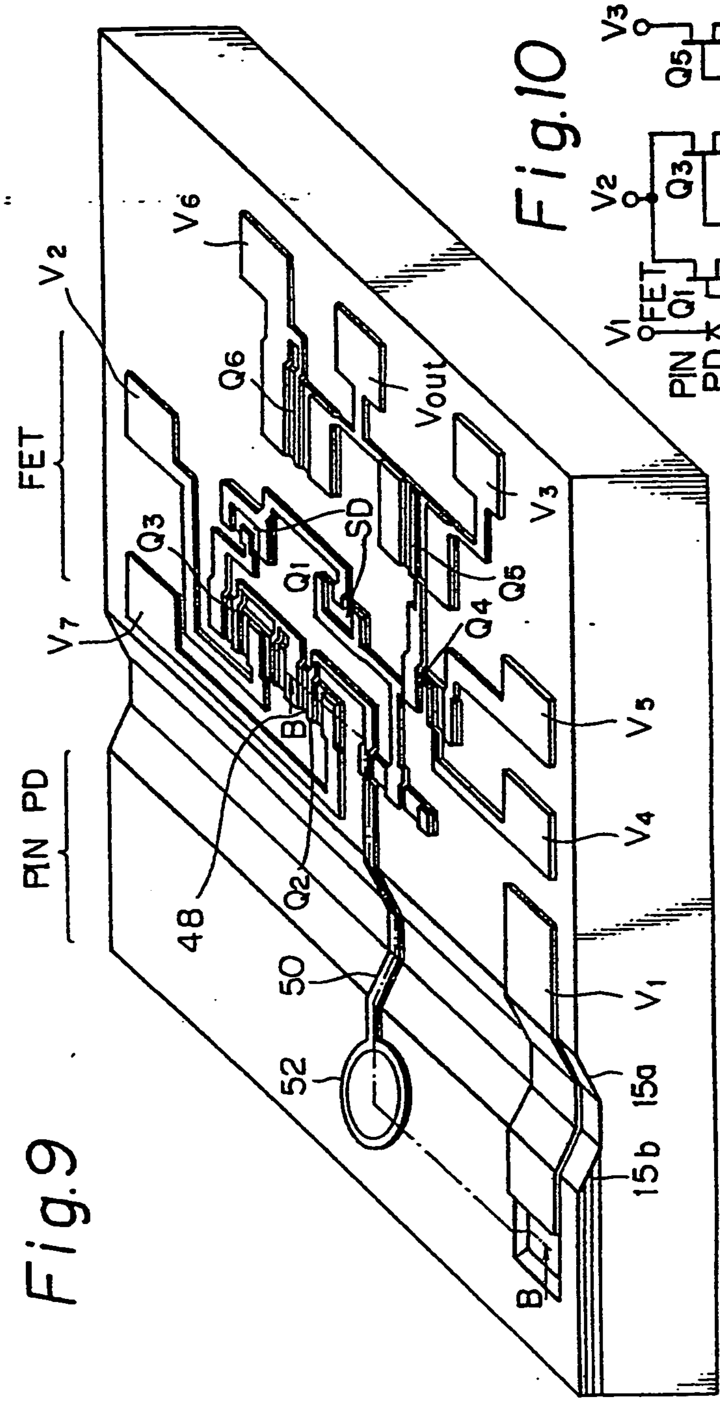


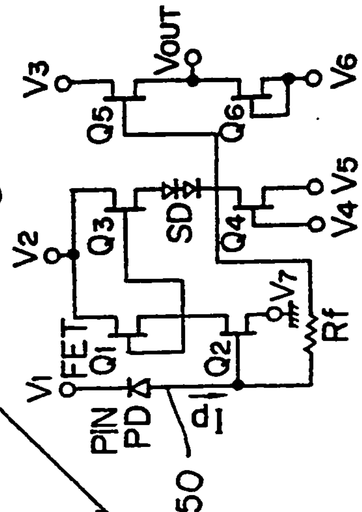
Fig.8





FET
PIN PD
V2
V6
V7
Q3
Q1
Q6
Q5
Q4
Q2
SD
Vout
V3
V5
V4
V1
B
48
50
52
15a
15b

Fig.9



V3
VOUT
V6
Q5
Q6
V2
Q3
SD
Q4
V4 V5
V1
FET
Q1
Q2
V7
Rf
PIN
PD
50

Fig.10

Fig.11A

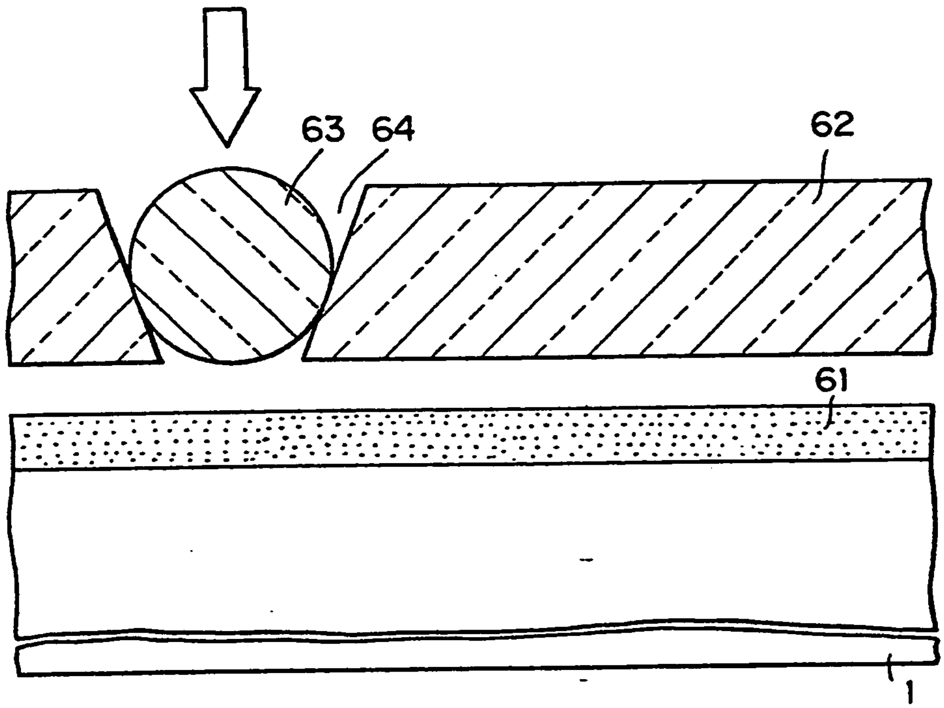


Fig.11B

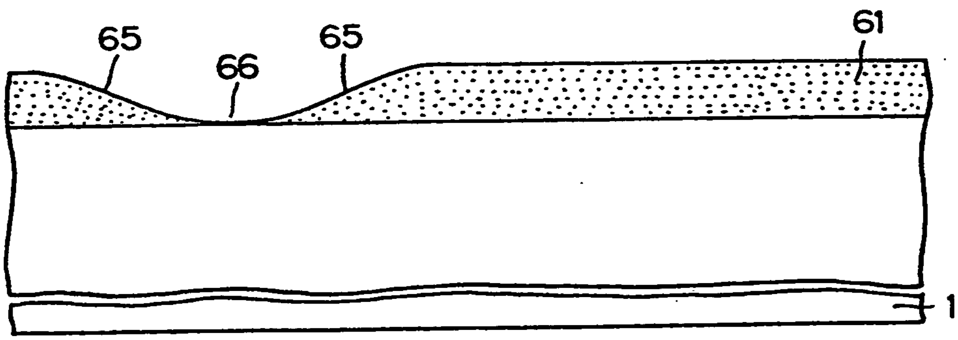


Fig.12A

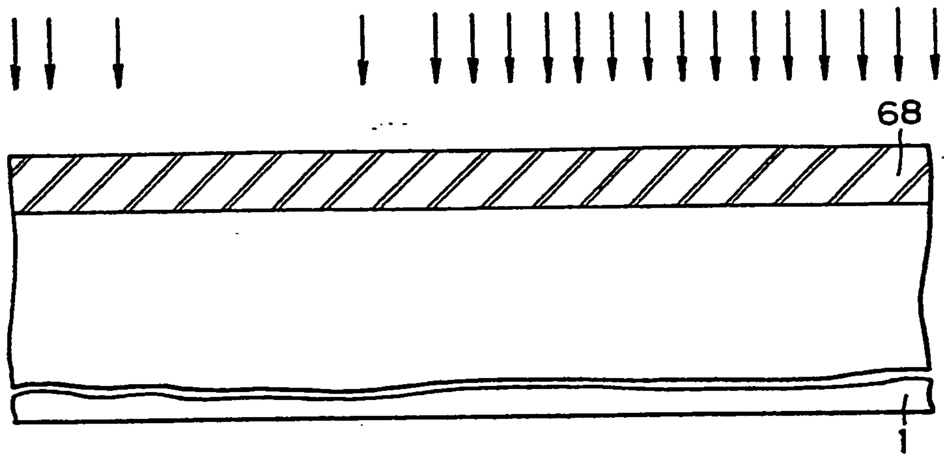


Fig.12B

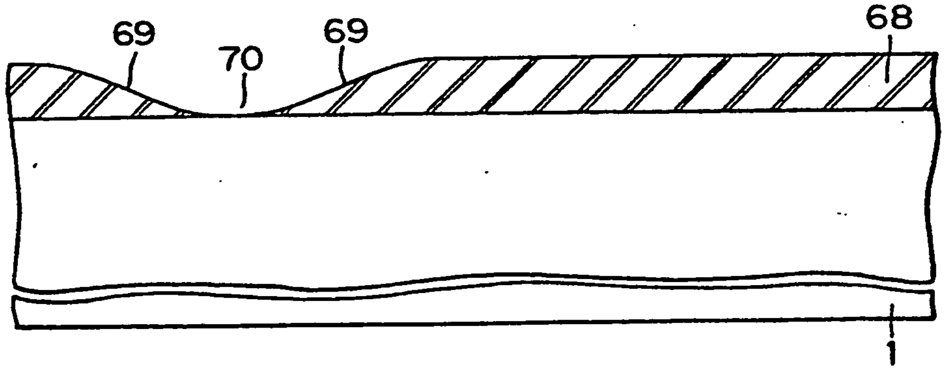


Fig.13A

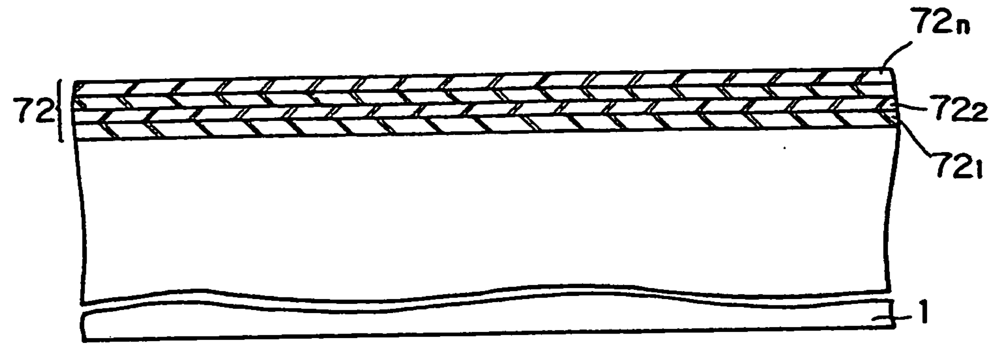


Fig.13B